CLAIMS

What is claimed is:

1. A readout circuit unit cell for use with a radiation detector, comprising a plurality of capacitances, switches and transistors that are programmably coupled together to form one of a first amplifier circuit having a first gain state or a second amplifier circuit having a second gain state that differs from the first gain state.

2. A readout circuit unit cell as in claim 1, where said first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit.

3. A readout circuit unit cell as in claim 2, where the first gain state is wider than the second gain state.

4. A readout circuit unit cell as in claim 1, where the first gain state overlaps the second gain state.

5. A readout circuit unit cell as in claim 1, where said plurality of capacitances, switches and transistors are programmably coupled together to form said first amplifier circuit below an illumination level threshold, and are programmably coupled together to form said second amplifier circuit above said illumination level threshold.

6. A readout circuit unit cell as in claim 1, comprising a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit.

7. A readout circuit unit cell as in claim 2, where said SFD input circuit operates in one of at least two integration modes: a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode.

8. A readout circuit unit cell as in claim 2, where one of said transistors is configured when operating in a CTIA mode to function as a current source for a CTIA amplifier, and operates as a reset switch when operating in a SFD mode.

9. A method to operate a readout circuit unit cell with a radiation detector, comprising:

providing the readout circuit unit cell to have a plurality of components that comprise capacitors, switches and transistors; and

coupling together said plurality of components in a first mode of operation to form a first photocurrent amplifier circuit having a first gain state, and in a second mode of operation to form a second photocurrent amplifier circuit having a second gain state that differs from the first gain state.

10. A method as in claim 9, where said first amplifier circuit is comprised of a Charge Transimpedance Amplifier (CTIA) input circuit, and where said second amplifier circuit is comprised of a Source Follower per Detector (SFD) input circuit.

11. A method as in claim 10, where the first gain state is wider than the second gain state.

12. A method as in claim 9, where the first gain state overlaps the second gain state.

13. A method as in claim 9, where said plurality of capacitances, switches and transistors are coupled together to form said first amplifier circuit below an illumination level threshold, and are coupled together to form said second amplifier circuit above said illumination level threshold.

14. A method as in claim 9, where said plurality of capacitances, switches and transistors comprise a sample/hold circuit for coupling the unit cell to an output bus, where said sample/hold circuit comprises said SFD input circuit.

15. A method as in claim 10, comprising operating said SFD input circuit in one of at least two integration modes: a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode.

16. A method as in claim 10, where one of said transistors is configured when operating in a CTIA mode to function as a current source for a CTIA amplifier, and operates as a reset switch when operating in a SFD mode.

17. A readout circuit unit cell for use with an infrared (IR) radiation detector, comprising a plurality of capacitances, switches and transistors that are controllably coupled together to form, in a first mode of operation below an illumination level threshold, a CTIA input circuit, and to form, in a second mode of operation above the illumination level threshold, a lower gain SFD input circuit.

18. A readout circuit unit cell as in claim 17, comprising a sample/hold circuit for coupling the unit cell to a column amplifier via a column output bus, where said sample/hold circuit comprises said SFD input circuit.

19. A readout circuit unit cell as in claim 17, where said SFD input circuit operates in one of at least two integration modes: a snapshot integrate-then-read (ITR) mode and a progressive scan integrate-while-read (IWR) mode.

20. A readout circuit unit cell as in claim 17, where one of said transistors is configured when operating in a CTIA mode to function as a current source for a CTIA amplifier, and operates as an integration reset switch when operating in a SFD mode.